

ABSTRACT

A power semiconductor device has an active region that includes a drift region. At least a portion of the drift region is provided in a membrane which has opposed top and bottom surfaces. In one embodiment, the top surface of the membrane has electrical terminals connected directly or indirectly thereto to allow a voltage to be applied laterally across the drift region. In another embodiment, at least one electrical terminal is connected directly or indirectly to the top surface and at least one electrical terminal is connected directly or indirectly to the bottom surface to allow a voltage to be applied vertically across the drift region. In each of these embodiments, the bottom surface of the membrane does not have a semiconductor substrate positioned adjacent thereto.